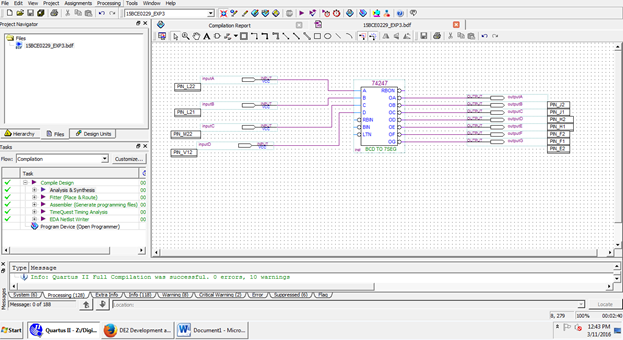
**Experiment: 6**

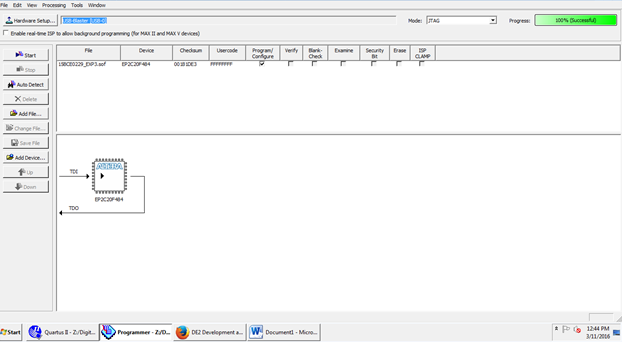
Name: VOLETI RAVI

Reg no: 15BCE0082

1. **AIM:** To design the BCD to seven segment circuit (use seven segment display to show the output)

**BLOCK DIAGRAM -**





**TRUTH TABLE -**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | A | B | C | D | a | b | c | d | e | f | g |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 2 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 4 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 6 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 7 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

**EXPRESSIONS:**

a = A + C + B’C + B’D’

b = B’ + C’D + CD

c = B + C’ + D

d = B’D’ + CD’ + BC’D + BC + A

e = B’D’ + CD’

f = A + C’D’ + BC’ + BD’

g = B’C + CD’ + BC’ + A

1. **Aim:** Design a circuit to display thrice of a number on seven segment display (Consider maximum input number to be 2 bit)

**Truth table:**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Digit | Output | X | Y | A | B | C | D | E | F | G | h |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 3 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 2 | 6 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3 | 9 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

**OUTPUT:**

C=D=A=X+X’

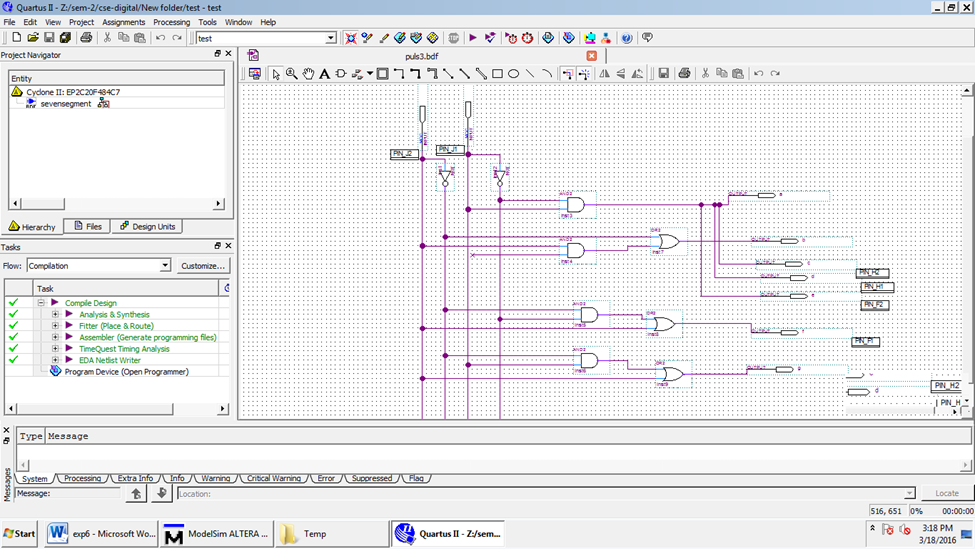
B=X’+XY

E=B’

F=A’B’+A

G=A’B+A

**DIAGRAM:**

****

1. **AIM:** Design a combinational circuit which converts 2 4 2 1 code to 8 4 -2 -1 code

**TRUTH TABLE:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **2** | **4** | **2** | **1** | **Minterm** | **8** | **4** | **-2** | **-1** |
| **A** | **B** | **C** | **D** |  | **W** | **X** | **Y** | **Z** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 3 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 4 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 5 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 12 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 13 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 14 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 15 | 1 | 1 | 1 | 1 |

**DON’T CARE CASES:** 6,7,8,9,10,11

**Expression:**

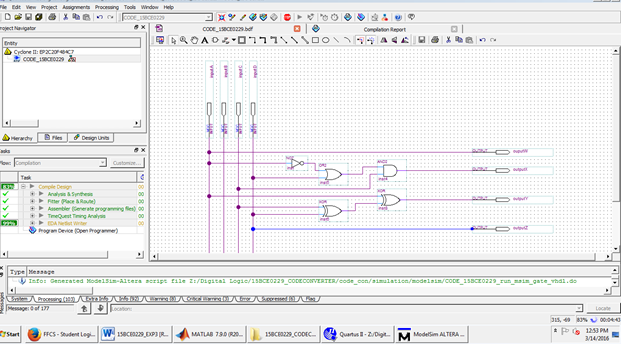
**W=A**

X=+D)C

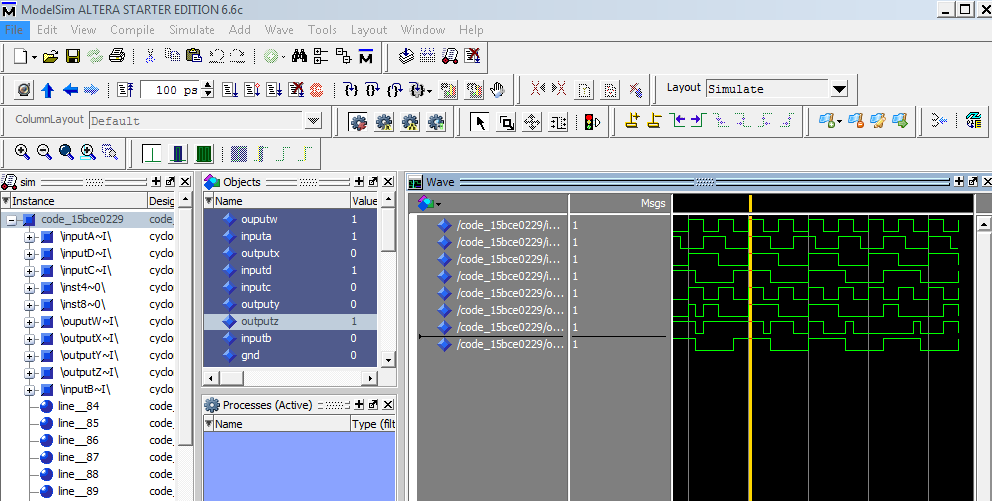
Y=)

Z=D

**BLOCK DIAGRAM:**

****

**WAVE OUTPUT-**



1. **AIM:** A circuit has four inputs RSTU and four outputs VWYZ. RSTU represents a binary coded decimal digit. VW represents the quotient and YZ the remainder when RSTU is divided by 3 (VW and YZ represent 2-bit binary numbers). Assume that invalid inputs do not occur. Design a code converter which converts RSTU to VWYZ.

**TRUTH TABLE:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| X | Y | A | B | C | D | E | F | G |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

**Output:**

1.B= XY’

2. D= XY

3. E=Y

4. F=X’Y

5. G=X’Y’

**OUTPUT:**

